The anabrid CMOS Multiplier

Anabrid is a pioneer in future analog-digital mixed signal information processing, being performant, energy efficient and at unmatched flexibility. The common unique value proposition (UVP) is the 65nm CMOS technology base which is affordable and allows for combining various analog and digital CMOS IP blocks on a single chip, saving production costs and precious space in appliances.

Anabrid holds a patent on the world's first analog multiplier in CMOS technology. While it is a cricital key component of our planned analog computer on chip, it will also be an early side product and cash cow starting in 2025.

This whitepaper features this standalone analog multiplier chip and presents the buisness case.

Market overview

Target Market	Total Available Market	Market Players
The global multiplier market was valued at USD 1,132.2 million in 2021 and is expected to reach USD 1,714.7 million by 2030, at a CAGR of 4.8%.	During the forecast period 2022-2027, the analogue integrated circuits market, valued at US$ 73. 89 billion in 2021, is expected to grow at a CAGR of 7.28%.	Only two existing sellers of multiplier chips: Analog Devices (eg. AD663), Texas Instruments (eg. MPY634)

Technological features of our new product

Superiority	Integration	Flexibility
Our chip requires less power then comparable circuits and has superiour technological features in terms of high linearity and bandwith.	It allows for easy integration on existing CMOS technology (System on chips) in contrast to existing products (bipolar technology). This allows for higher integration and more powerful analog I/O in microcontroller (MCU) appliances.	The design can be easily extended to compute more advanced functions such as Z=X1*Y+X2*Y+X3*Y. That allows the saving of discrete components in circuits and more advanced uses.

Customers and Channels

Selling discrete electronics	Exemplaric industrial application domains	Drivers and Opportunity
In traditional industry contexts (that means outside of consumer electronics and IT), the quantities are not so high that application specific ICs (ASICs) can be developed economically for a problem; in these areas, the components are also not so cost-sensitive, i.e. higher margins are possible.	• Sensors and actuators in energy supply systems • Environmental measurement technology and safety systems • Industrial automation and monitoring • Transport systems, traffic management and monitoring	• Increasing demand for frequency multipliers in communication and radar applications. • Growing popularity of frequency multipliers in wireless infrastructures and base stations. • Increasing demand for frequency multipliers in the automotive industry. The spread of 5G technology and its increasing acceptance in various industries.

Realization and Revenue Streams

- The first variant will be a SoC compatible (1.2V, 65nm) chip supposed to be sold in licenses (CMOS IP) at typical net prices of €150k. Customers are in the highly specialized CMOS chip market who design and sell ASICs. The estimated yearly revenue is in the order of €5M.
- The second (follow-up) variant will be a high voltage (5V, 350nm) chip that can be used as a standalone product (drop-in solution / concurrency to existing products such as analog devices AD836). This will be an off-the-shelf-product sold by various standard electronics distributors. The customers are the same of the global electronics components industry. They have a need of building standard electronics for signal processing and either sell their hardware or produce it for self-use. The estimated yearly revenue are between €10M and €200M.

We already started the realization of this chip in 65nm in a self-funded manner. In this document, we mainly focus on the standalone product.

Cost Structure and Pricing

The multipilier stand-alone IC 5V single supply with OTP memory calibration chip project is scheuled for 24 person months (IC design and layout). We schedule two shuttles MPW at Europractice. The overall non recurring development costs are 402,000€.

We then determine the full costs per chip to 1,15€ with conservative assumptions which are within our means (12 inch wafers, 295mm area, 10 mm² die size, 75% net yield, 20pin SOIC housing, final size of 100k good dies per batch, including testing and logistics). These costs can be reduced by a factor of 10 with efficient mass production.

In contrast, prices for existing products are in the range of 10-20€, yet being technologically inferior. That means we will be competitive with simple means.